# STRUCTURE OF A FLASH MEMORY

## CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90110698, filed May 4, 2001.

## BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to structure of a memory, and in particular, a structure of a flash memory.

Description of the Prior Art

In recent years, as a result of high demand of portable electronic appliances, there has been a great increase in demand for flash memories. The manufacturing technology of a flash memory has gradually matured and developed. Thus, the cost of production has been lowered and in turn, purchasing activities will be stimulated and new applications of a flash memory will be developed. The recently developed electrically erasable and program ROM has a faster storage speed. Therefore, it has been widely used in film for digital cameras, memory for PDA, MP3 players, electronic answering devices, programmable ICs, etc, which are the market applications of a flash memory.

A conventional flash memory employs doped polycrystalline silicon to manufacture a floating gate and a control gate. When the memory proceeds to program, appropriate program voltages are respectively added to the source region, the drain

region and the control gate. Electrons flow from the source region to the drain via channel. In this process, some of the electrons will pass through the tunneling oxide layer beneath the polycrystalline silicon floating gate layer and enter into and distribute evenly throughout the entire polycrystalline floating gate layer. The phenomenon of electrons passing through the oxide layer into the polycrystalline floating gate is known as the tunneling effect. This tunneling effect can be further classified into two different situations, Channel Hot-Electron Injection and Fowler-Nordheim Tunneling (F-N Tunneling). Generally, a flash memory is programmed by way of Channel Hot-Electron Injection and passes though the side of the source, or the channel region is erased by F-N Tunneling. However, if a weak point exists at the tunneling oxide layer beneath the polycrystalline silicon floating gate, current leakage of the memory element can easily occurr, which affects the reliability of the memory element.

In order to solve the problem of current leakage within the flash memory element, a recent method that has been developed is the formation of a charge trapping layer on the substrate. The material for the charge trapping layer is a stacked structure of SiO2/Si3N4/SiO2 (Oxide-Nitride-Oxide) (abbreviated as ONO) complex layers, and source region and drain regions are formed subsequently on the substrate of the two lateral sides of the ONO layer.

The silicon nitride layer of the ONO charge trapping layer has a charge gripping effect, so the electrons injected to the ONO layer will not evenly distribute on the entire silicon nitride but are concentrated on only a portion of the silicon nitride by way of Gaussian distribution. Thus, the sensitivity on the weak point of the oxide layer is low and current leakage will not occur easily. As silicon nitride layer of the charge trapping

layer is the essentially layer to grip electrons, this memory cell is known as Silicon Nitride Read Only Memory (NROM).

Additionally, the advantage of the ONO charge trapping layer is that the electrons will only approach the tunnel at the top section of the source or drain for partial storage during element programming. Thus, in the course of the program, the source/drain region and the gate can be respectively applied with voltage, and when approaching the silicon nitride layer at the other end of the source/drain region, Gaussian distributed electrons are generated. Thus, by changing the application of the voltage at the gate and the two lateral sides of the source/drain region, a single ONO charge trapping layer can have two electrons with Gaussian distribution, a single electron with Gaussian distribution, or no electrons. Thus, if silicon nitride is used as a material for a flash memory of the charge trapping layer, four kinds of states can be written to a single memory cell, thus forming a 1 cell 2 bit flash memory.

However, as the number of programming/erasing operations of the memory increases, damage on the silicon oxide of the ONO will become more serious, leading to a change in threshold voltage (denoted by $V_{th}$). As the change of threshold voltage increases, the leakage of electrons is increased, and the data retention of the memory is reduced. Thus, minimizing the variation of threshold voltage is an imperative issue.

## SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a structure of a flash memory, which reduces the amount of variation of the threshold voltage and enhances data retention of the flash memory.

It is another object of the present invention is to provide a structure of a flash memory comprising an electron trapping layer, a gate and a source/drain region, wherein the electron trapping layer is formed by stacking in sequence a first oxide layer and a dielectric layer with a high dielectric constant. The gate is arranged on the electron trapping layer, and the source/drain region is arranged on the substrate of the two lateral sides of the electron trapping layer. In addition, the band gap of the material used for the high dielectric constant dielectric layer determines whether or not a second oxide layer should be provided on the high dielectric constant dielectric layer. The second oxide layer is not needed if the band gap of the high dielectric constant dielectric layer is closer to or greater than that of silicon oxide. On the other hand, a second oxide layer is needed if the band gap is smaller than that of silicon oxide.

In the present invention, a material with a high dielectric constant refers to a material with a dielectric constant higher than that of $Si_3N_4/SiO_2$ (also known as NO), so such a term in the present invention is not a formal term. The band gap refers to the gap between two tolerable electron energy bands of metal and semiconductor.

The advantage of the present invention is that a high dielectric constant material is used as the main material for the dielectric layer. Thus, the amount of variation of the threshold voltage is greatly reduced, and data retention of the flash memory is enhanced.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

Fig. 1 is a cross-sectional view of a preferred embodiment of the flash memory of the present invention.

## DETAILED DESCRIPTION OF THE PRESENT INVENTION

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

The present invention provides a structure of a flash memory which reduces the variation of the threshold voltage to a minimum. Fig. 1 is a cross-sectional view of a preferred embodiment of the flash memory of the present invention.

As shown in Fig. 1, the flash memory comprises an electron trapping layer 112, a gate 108 and a source/drain region 110. The gate 108 is located on the electron trapping layer 112, and the source/drain region 110 is positioned at the two lateral sides of a substrate 100. The electron trapping layer 112 is formed by stackinga first oxide layer 102 and a dielectric layer 104. The dielectric layer 104 is made from a material with a high dielectric constant.

In accordance with the present invention, the material of the dielectric layer 104 of the electron trapping layer 112 requires a high dielectric constant ( $\varepsilon$ ). The reason for

using a material with a high dielectric constant is shown by the relationship of the threshold voltage being varied with respect to time (denoted by $\Delta V_{th}(t)$) and the dielectric constant, as follows:

$$\Delta V_{th}(t) = -2.3 \frac{\overline{t_{ONO}}}{\varepsilon_{ONO}} \propto \frac{\bar{q}\bar{n}N_{DX}}{2\sqrt{2mE_{to}}} \times \log t$$

where $\varepsilon_{ONO}$ is the dielectric constant of the ONO layer;

$E_{to}$ is the Oxide Trap Energy; and

$qN_{DX}$ is the Trap Charge Density.

Accordingly, the dielectric constant of the dielectric layer 104 for the electron trapping layer 112 has to be upgraded in order to reduce the amount of variation $\Delta V_{th}(t)$ of the threshold voltage. The flash memory structure of the present invention employs a material having a high dielectric constant when manufacturing the electron trapping layer 112 in order to reduce the amount of variation of the threshold voltage. Thus, the data retention of the flash memory is enhanced.

The first oxide layer 102 of the electron trapping layer 112 is used to enhance adsorption force between the substrate 100 and the high dielectric constant dielectric layer 104 and to avoid the formation of a defect. Additionally, as shown in Fig. 1, the electron trapping layer 112 further comprises a second oxide layer 106 on the dielectric layer 104 made from a high dielectric constant material, wherein the second oxide layer 106 is used to enhance the adsorption force between the high dielectric constant dielectric layer 104 and the gate 108 formed subsequently thereon and to avoid the formation of a defect.

In the present invention, a material having high dielectric constant refers to a material with a dielectric constant higher than that of $Si_3N_4/SiO_2$ (also known as NO). The materials for the high dielectric constant layer 104 are, for example, $Al_2O_3$, $Y_2O_3$, $ZrSi_xO_y$, $HfSi_xO_y$, $La_2O_3$, $ZrO_2$, $HfO_2$, $Ta_2O_5$, $Pr_2O_3$ and $TiO_2$.

The following table 1 shows the dielectric constants of the above-mentioned high-dielectric constant materials, also including $Si_3N_4/SiO_2$, $SiO_2$ and $Si_3N_4$.

| Materials | Dielectric Constant |
|---|---|
| $SiO_2$ | 2-9 |
| $Si_3N_4$ | 7.5 |
| NO ($Si_3N_4/SiO_2$) | 7-8 |
| $Al_2O_3$ | 10 |
| $Y_2O_3$ | 12-14 |
| $ZrSi_xO_y$ | 12-22 |
| $HfSi_xO_y$ | 15-25 |
| $La_2O_3$ | 20 |
| $ZrO_2$ | 22 |
| $HfO_2$ | 25 |
| $Ta_2O_5$ | 26 |
| $Pr_2O_3$ | 31 |
| $TiO_2$ | 80 |

Table 1

As shown in Table 1, the dielectric constant of the high dielectric constant material of the present invention is higher than 8, which is the dielectric constant for

$Si_3N_4/SiO_2$. In addition, the high dielectric constant dielectric layer 104 of the present preferred embodiment can be, for example, a mixture of the above-mentioned high dielectric constant dielectric materials or a stack layer of the above-mentioned high dielectric constant materials. Due to the fact that high dielectric constant material is used as the material for the dielectric layer, the variation of the threshold voltage is greatly reduced, and in turn, the data retention of the flash memory is enhanced.

In addition, the band gap of the material of the high dielectric constant dielectric layer 104 determines whether or not a second oxide layer 106 should be provided to the high dielectric constant layer 104. The second oxide layer 106 is not needed if the band gap of the dielectric layer 104 is closer to or greater than that of silicon oxide. On the other hand, the second oxide layer 106 is needed if the band gap is smaller than that of silicon oxide. Table 2 shows the band gap of the materials used for the dielectric layer 104 in the preferred embodiment of the present invention. The band gaps of $SiO_2$ and $Si_3N_4$ are also shown in Table 2.

| Materials | Band Gap (eV) |
|---|---|
| $SiO_2$ | 9 |
| $Si_3N_4$ | 5.3 |
| $Al_2O_3$ | 8.0 |
| $Y_2O_3$ | 5.6 |
| $ZrSi_xO_y$ | 6.5 |
| $HfSi_xO_y$ | 6.5 |
| $La_2O_3$ | 4 |
| $ZrO_2$ | 7.8 |
| $HfO_2$ | 6 |

| | |
|---|---|
| $Ta_2O_5$ | 4.4 |
| $Pr_2O_3$ | - |
| $TiO_2$ | 2.3 |

Table 2

If the band gap of the dielectric layer 104 is close to or larger than that of the conventional $SiO_2$ layer, then the dielectric layer 104 can be substituted for the conventional oxide layer formed on the dielectric layer and can have identical effects.

The present invention is characterized in that a high dielectric constant material is used as a main material for the dielectric layer. Accordingly, the variation of the threshold voltage is greatly reduced, and in turn, the data retention of the flash memory is enhanced. Thus, the effectiveness of the flash memory is greatly improved, thereby increasing efficiency and speed.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.